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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,878	08/23/2001	Hidetaka Magoshi	SCEA 3.0-003	1362

530 7590 06/27/2005

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,878	MAGOSHI, HIDETAKA	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4, 5, 9-11, 23, 26-30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Blomgren et al., US Patent 5,781,750, cited by Applicant on the Information Disclosure Statement filed on January 13, 2003.

3. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action mailed on January 12, 2005.

4. Claims 35-37 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Blomgren et al., US Patent 5,781,750, cited by Applicant on the Information Disclosure Statement filed on January 13, 2003.

5. Referring to claim 35, Blomgren et al. have taught a system for processing a computer instruction from a source of such instructions, the system comprising:

a. a complex instruction detector being operable to accept computer instructions from the source and to determine whether each instruction is a complex instruction on an instruction by instruction basis (Figure 2, elements 42 and 38, column 6, lines 28-32, column 7, lines 1-12 and 25-67, column 9, lines 1-32 and 45-54, Each instruction is decoded and on a TLB miss or an unknown opcode, emulation mode is entered. An embodiment that is taught by Blomgren is to directly support the simple instructions and

to emulate the complex instructions, see column 7, lines 1-12 and column 9, lines 45-54. In this embodiment, for each instruction a decoder determines when an instruction is complex.);

b. an address generator being operable to accept computer instructions from the source and to output an address for each of the computer instructions based on the respective computer instruction (column 7, lines 36-42);

c. a jump instruction generator in operative communication with the address generator, the jump instruction generator being operable to output an instruction to jump to the address from the address generator (column 7, lines 36-42, The jump instruction is loaded into the instruction pointer.); and

d. an instruction selector in operative communication with the jump instruction generator, the source, and the complex instruction detector, the instruction selector being operable to output either the computer instruction from the source or the instruction from the jump instruction generator depending upon the determination by the complex instruction detector (Figure 2, element 46, column 6, lines 53-56).

6. Referring to claim 36, Blomgren et al. have taught a method of executing a program with a processor, the processor being capable of executing a set of instructions, the method comprising:

a. providing an original instruction from a sequence of instructions comprising a program stored in a memory (column 2, lines 8-12);

b. generating an address from the original instruction (column 7, lines 36-42);

c. generating a jump and link instruction to the address (Column 7, lines 36-42),

d. the jump and link instruction comprising an instruction for the processor to execute instructions at the address and then return to the instruction following the original instruction in the program (column 5, lines 53-67);

e. determining whether the original instruction is a complex instruction on an instruction by instruction basis (Figure 2, elements 42 and 38, column 6, lines 28-32, column 7, lines 1-12 and 25-67, column 9, lines 1-32 and 45-54, Each instruction is decoded and on a TLB miss or an unknown opcode, emulation mode is entered. An embodiment that is taught by Blomgren is to directly support the simple instructions and to emulate the complex instructions, see column 7, lines 1-12 and column 9, lines 45-54. In this embodiment, for each instruction a decoder determines when an instruction is complex.); and

f. selecting the jump and link instruction or the original instruction based on the result of the determining (Figure 2, element 46, column 6, lines 53-56, elements 42 and 38, column 6, lines 28-32, column 7, lines 1-12 and 25-67, column 9, lines 1-32 and 45-54.).

2. Referring to claim 37, Blomgren et al. have taught a system for processing computer instructions between a memory and a processor, the system comprising:

a. a complex instruction detector operatively connected to the memory so as to receive computer instructions from the memory, the complex instruction detection being operable to output a value indicative of whether the instruction is a complex instruction on an instruction by instruction basis (Figure 2, elements 42 and 38, column 6, lines 28-32, column 7, lines 1-12 and 25-67, column 9, lines 1-32 and 45-54, Each instruction is

decoded and on a TLB miss or an unknown opcode, emulation mode is entered. An embodiment that is taught by Blomgren is to directly support the simple instructions and to emulate the complex instructions, see column 7, lines 1-12 and column 9, lines 45-54. In this embodiment, for each instruction a decoder determines when an instruction is complex.);

b. an address generator operatively connected to the memory so as to receive computer instructions, the address generator being operable to generate an address (column 7, lines 36-42);

c. a jump instruction generator operatively connected to the address generator (column 7, lines 36-42);

d. an instruction selector operatively connected to the jump instruction generator, the memory, the complex instruction detector, and the processor (figure 2, element 46, column 6, lines 53-56) so as to receive jump instructions from the jump instruction generator (Figure 2, element 46, column 6, lines 53-56), computer instructions from the memory (Figure 2, element 46, column 6, lines 53-56), and the value from the complex instruction detector, whereby depending on the value from the complex instruction detector, either the jump instruction or the computer instruction is provided by the instruction selector to the processor (Figure 2, elements 38, 42, and 46, column 6, lines 53-56).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15-22, 31, 33, ad 34 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, cited by Applicant on the Information Disclosure Statement filed on January 13, 2003, in view of Hennessy.

4. Claims 6, 7, 8, 12, 13, and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, cited by Applicant on the Information Disclosure Statement filed on January 13, 2003.

5. Claims 3, 24, and 25 are rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, in view of Ireton, US Patent 5,826,089, both cited by Applicant on the Information Disclosure Statement filed on January 13, 2003.

6. Claim 32 is rejected under 35 U.S.C. 103(a) as being obvious over Blomgren et al., US Patent 5,781,750, in view of Ireton, US Patent 5,826,089, both cited by Applicant on the Information Disclosure Statement filed on January 13, 2003, and further in view of Hennessy.

7. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action mailed on January 12, 2005.

Response to Arguments

8. On page 13, Applicant argues in essence:

> *"Blomgren is not selecting jump instructions based on whether an instruction is a member of a set of instructions, but rather based upon a bit flag set by a programmer or the like."*

However, Blomgren has taught selecting a jump instruction based on whether an instruction is a member of a set of instructions. In Blomgren, an instruction is decoded and it is determined whether the instruction is a complex instruction. (Figure 2, elements 42 and 38, column 6, lines 28-32, column 7, lines 1-12 and 25-67, column 9, lines 1-32 and 45-54). Each instruction is decoded and on a TLB miss or an unknown opcode, emulation mode is entered. An embodiment that is taught by Blomgren is to directly support the simple instructions and to emulate the complex instructions, see column 7, lines 1-12 and column 9, lines 45-54. In this embodiment, for each instruction a decoder determines when an instruction is complex. When the instruction is determined to be complex, then the jump instruction is selected and executed to emulate the complex instruction. Therefore, Blomgren has in fact taught selecting a jump instruction based on whether an instruction is a member of a set of instructions. Therefore this argument is moot.

9. On pages 13 and 14, Applicant argues in essence:

"Blomgren neither teaches nor suggests determining whether an instruction is a member of a set of instructions and selecting between an "original" instruction and a "jump" instruction based upon the determination."

However, Blomgren has in fact taught determining whether an instruction is a member of a set of instructions, see the argument above. Blomgren has also taught selecting between an "original" instruction and a "jump" instruction based upon the determination. When a complex instruction is encountered, an instruction is selected to cause the processor to jump to a routine to emulate the original complex code. Therefore this argument is moot.

10. On pages 15 and 16, Applicant argues in essence:

"The combination does not result in the claimed invention. ... The parallel pipelining discussed in Hennessy only teaches how to pipeline across multiple straight-line code sequences with no branches. It does not teach or suggest processing jump instructions or selecting between a jump instruction and a complex instruction. Thus Hennessy cannot remedy the deficiencies of Blomgren. ... Also there is no teaching or suggestion as to how Blomgren could be redesigned to incorporate the "instruction level parallelism" of Hennessy."

However, that fact that Hennessy may not teach the concept of processing jump instructions or selecting between a jump instruction and a complex instruction is irrelevant as Hennessy has not been cited for that concept. Hennessy has been cited for teaching the concept that increasing parallelism, in general, increases overall performance and instruction throughput of the system. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of Blomgren et al. determine whether the computer instruction is complex in parallel with the steps of generating the address and generating the jump instruction for the desirable purpose of increasing the overall performance and instruction throughput of the system (Hennessy, pages 221-223). Therefore this argument is moot.

11. On pages 15-17, Applicant argues in essence:

"There is no motivation to combine the references to arrive at the invention. ...As acknowledged in the office action, Blomgren does not teach the parallel processes required by claims 15 and 31. As stated above, one would have to physically alter the processing system of Blomgren to enable parallel processing. The fact that a prior art process or device could be modified so as to produce the claimed invention is not a basis for an obviousness rejection unless the prior art suggests the desirability of such modification."

However, In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the system of Blomgren et al. determine whether the computer instruction is complex in parallel with the steps of generating the address and generating the jump instruction for the desirable purpose of increasing the overall performance and instruction throughput of the system, as suggested by Hennessy (Hennessy, pages 221-223). Therefore this argument is moot.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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